REMARKS

The Office Action dated June 18, 2003 has been carefully reviewed and the foregoing amendments made in response thereto. Reconsideration of the grounds of objections and rejections is respectfully requested in view of the above amendments and the remarks herein.

Summary of the Office Action

Claims 24-25, 27, 28, 42, 44 and 46 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Pat. No. 6,148,361 to Carpenter et al. Claim 41 stands rejected under 35 U.S.C. § 103(a) as being unpatentable in view of Carpenter. Claims 26, 29-32, 36, 37, 39, 40, 43, 45, 47-49 stand rejected under 35 U.S.C. § 103(a) as being unpatentable in view of Carpenter further in view of U.S. Pat. No. 4,462,075 to Mori et al. Claims 33-35 and 38 stand rejected under 35 U.S.C. § 103(a) as being unpatentable in view of Carpenter and Mori further in view of U.S. Pat. No. 5,214,652 to Sutton.

The Rejection Under 35 USC 102(e)

In the Office Action, the Examiner asserts that Carpenter teaches a process for assigning tasks to a queue in a multiprocessor digital data processing system having a preemptive operating system at Col. 3, lines 1-58 through Col. 8 lines 5-63. However, Carpenter is directed to an interrupt architecture for efficiently processing *interrupts* in NUMA type systems, while the subject invention is directed to an architecture for efficiently routing *tasks* to processor groups in a multiprocessor system. The claims have been amended to more clearly distinguish the "elementary task queue" of the present invention from the cited prior art.

Carpenter discloses partitioning nodes (modules) into external interrupt domains so that an external interrupt is always presented to the processor within the external interrupt domain in which the interrupt occurs, thereby reducing the amount of NUMA internode processing required to process an interrupt. The system in Carpenter is directed to efficient interrupt routing in large-scale NUMA computer systems. On the other hand, the subject invention is directed to efficient routing of *tasks* in a multi-processor system, and is not at all related to the processing of interrupts. Carpenter does not teach or suggest a task routing architecture that utilizes multiple *task queues*.

A process for routing interrupts is NOT the same as creating and managing multiple task queues, as an interrupt is completely different from a task. As described at Col. 1, lines 14-19, "interrupts are often utilized to alert a processor to the occurrence of an event that requires special handling." Tasks, on the other hand, as described in the present specification at page 1, line 22 through page 2, and page 6, lines 9-11, are threads of a process that are executed in parallel in a multiprocessor system. Tasks are executed to implement a process, such as a computer application. Interrupts are used to handle errors or communicate information between devices. The Carpenter reference acknowledges this difference at Col. 8, lines 46-62 - current task priority registers in the Carpenter system indicate "the relative task priority of the current task when no interrupts are being serviced." Clearly, tasks and interrupts are not equivalent.

Assuming, arguendo, that "tasks" and "interrupts" could be considered "equivalent", nevertheless equivalence and obviousness are not the same.) *In re Flint*, 141 USPQ 299 (C.C.P.A 1964). Indeed, a function of the Patent Laws is to stir inventors into reliance of patented disclosures to develop improved systems that perform equivalent

functions in a better way. When there is no suggestion in the prior art to the desirability of the structure, the improvement cannot be held to be obvious in view of the disclosure. *In re Randol* (C.C.P.A 1970).

In addition, even if interrupts could be analogized to tasks, the Examiner does not specify where in the Carpenter reference that multiple task queues are disclosed. While Carpenter discloses a "pending queue 130" for storing pending interrupts for a processor, a pending queue is only associated with one processor. As is clearly shown in Fig. 4 of the present invention, a task queue (51, 5b, 5c) may be associated with multiple processors. For example, task queue 5a is associated with processor group Ga, which is comprised of processors 20a and 21a. .

In the present invention, elementary task queues, each associated with a group of processors, are used to optimize the assignment of tasks to processors in a multiprocessor system. There is no mention of any task, thread or job queue anywhere in Carpenter, much less multiple task queues.

The Rejection Under 35 USC 103(a)

Mori is directed to a job processing method for an information processing system that includes a plurality of information processing devices. In the disclosed method, every job is reliably processed, even if an abnormality occurs, by use of the remaining processing devices in the system. Mori discloses broadcasting jobs to every processing device in the system upon detection of a job by one processing device. The job is processed by a first processing device, and if an abnormality is detected in this first processing device by another processing device, Mori teaches that the job will be processed by an alternative processing device.

The Examiner states that Mori teaches determining the number of processors in each group and the number of groups for achieving the best performance of the system. A close review of the cited sections of Mori reveal no such teaching. 37 CFR 1.104(c)(2) requires that the pertinence of each reference, if not apparent, must be clearly explained." Applicant hereby respectfully requests that each of the elements recited in the claims and alleged to be found in Mori be specifically identified in the reference, should any of the claims now presented be rejected again based on Mori.

Not only do the cited references not teach or suggest all the claim limitations, there is no motivation to combine Carpenter with Mori, as they are directed in completely different arts, and one skilled in one art would not be motivated to combine the references. Carpenter is directed to efficiently routing interrupts in a multiprocessor system. Mori is directed to processing jobs in an information processing system that includes three or more information processing devices. Each information processing device is comprises of a transmission controller, an information processor and a plurality of I/O devices. The information processing device and the information processor are systems that are comprised of many components, including processors, as used in Carpenter. The "processor" in Carpenter is a computer hardware component. The "processor" in Mori is an information system comprised of many computer hardware components. The Applicant therefore respectfully requests that the rejection of claims 26, 29-32, 36, 37, 39, 40, 43, 45, 47-49.

Summary

Applicant respectfully requests favorable reconsideration of this application, as amended. Claims 25-49 are pending, with Claims 24 and 42 being independent claims.

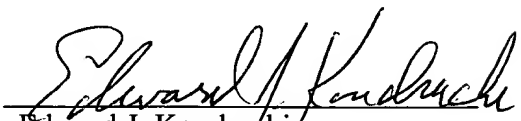
Should the Examiner believe that further amendments are necessary to place the application in condition for allowance, or if the Examiner believes that a personal interview would be advantageous in order to more expeditiously resolve any remaining issues, the Examiner is invited to contact Applicant's undersigned attorney at the telephone number listed below.

To the extent necessary, Applicant petitions for an extension of time under 37 CFR § 1.136. Please charge any shortage in fees due in connection with this application, including extension of time fees, to Deposit Account No. 50-1165 (Attorney Docket No T2147-906388) and credit any excess fees to the same Deposit Account.

Respectfully submitted,

Miles & Stockbridge P.C.

Date: October 17, 2003

By: 
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